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IN THE CLAIMS:

1. (currently amended) A ferroelectric transistor comprising:
- source and drain regions provided in a substrate; and
  - a gate structure on the substrate between the source and drain regions, the gate structure comprising
    - a conductive oxide layer overlying the substrate selected from the group of materials consisting of:
      - an oxide of the formula  $AO_x$ , where A is a material selected from the group consisting of Mo, W, Tc, ~~Re~~, ~~Ru~~, ~~Os~~, Rh, Ir, Pd, ~~Pt~~, In, Zn, Sn, Sr-Ru, Nd, Nb, Sm, La, V, and NaCl;
      - a perovskite oxide of the formula  $ABO_3$ , where A and B are a combination selected from the group consisting of (A = Ca, Sr)(B = V, Cr, Fe, Ru), (A = La)(B = Ti, Co, Ni, Cu), (A = H, Li, Na, K)(B = Re, Mo, Nb), and (A =  $La_{1-x}Sr_x$ )(B = V, Mn, Co);
      - a perovskite oxide of the formula  $A_2B_2O_7$ , where A and B are a combination selected from the group consisting of (A = Bi, Pd)(B =  $Ru_{1-x}Bi_x$ ,  $Ru_{1-x}Pb_x$ );
      - a layered perovskite oxide selected from the group consisting of  $CaTiO_3$ ,  $Ba_2RuO_4$ , and  $(Sr(Ru, Ir, Cr)O_3(SrO))_n$ ; and
      - a high temperature superconducting oxide selected from the group consisting of  $La_{1-x}Sr_xCuO_4$ ,  $Nd_{1-x}Ce_xCuO_4$ ,  $YBa_2Cu_3O_7$ ,  $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ , and  $(Nd_{1-x}Ce_x)_2CuO_4$ ;
      - a ferroelectric material layer overlying the conductive oxide layer, and

a top electrode conductive layer overlying the ferroelectric material layer.

2. (original) A ferroelectric transistor as in claim 1 further comprising a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

3. (original) A ferroelectric transistor as in claim 1 wherein the electrode conductive layer is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide.

4. canceled

5. (currently amended) A method of fabricating a ferroelectric transistor comprising the steps of:

preparing a semiconductor substrate;

forming a gate stack on the substrate, the gate stack comprising

a conductive oxide layer overlying the substrate selected from the group of materials consisting of:

an oxide of the formula  $AO_x$ , where A is a material selected from the group consisting of Mo, W, Tc, ~~Re~~, ~~Ru~~, Os, Rh, Ir, Pd, Pt, In, Zn, Sn, Sr-Ru, Nd, Nb, Sm, La, V, and NaCl;

a perovskite oxide of the formula  $ABO_3$ , where A and B are a combination selected from the group consisting of (A = Ca, Sr)(B = V, Cr, Fe, Ru), (A = La)(B = Ti, Co, Ni, Cu), (A = H, Li, Na, K)(B = Re, Mo, Nb), and (A =  $La_{1-x}Sr_x$ )(B = V, Mn, Co);

a perovskite oxide of the formula  $A_2B_2O_7$ , where A and B are a combination selected from the group consisting of (A = Bi, Pd)(B =  $Ru_{1-x}Bi_x$ ,  $Ru_{1-x}Pb_x$ );

a layered perovskite oxide selected from the group consisting of  $CaTiO_3$ ,  $Ba_2RuO_4$ , and  $(Sr(Ru, Ir, Cr)O_3(SrO)_N)$ ; and

a high temperature superconducting oxide selected from the group consisting of  $La_{1-x}Sr_xCuO_4$ ,  $Nd_{1-x}Ce_xCuO_4$ ,  $YBa_2Cu_3O_7$ ,  $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ , and  $(Nd_{1-x}Ce_x)_2CuO_4$ ;

a ferroelectric material layer over the conductive oxide layer;

and

a top electrode conductive layer over the ferroelectric material layer; and

forming drain and source regions on opposite sides of the gate stack.

6. (original) A method as in claim 5 wherein the gate stack further comprises a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

7. (original) A method as in claim 5 wherein the formation of the gate stack comprises the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack.

8. (original) A method as in claim 5 wherein the formation of the drain and source regions comprises the implantation to a high doping concentration.

9. (original) A method as in claim 5 further comprising the LDD ion implantation into the source and drain regions.

10. (original) A method as in claim 5 further comprising a dielectric spacer on the sidewall of the gate stack.

11. (original) A method as in claim 5 wherein the electrode conductive layer is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide.

12. canceled

13. (currently amended) A method of fabricating a ferroelectric memory transistor comprising:  
preparing a semiconductor substrate;  
forming a replacement gate stack on the substrate, the replacement gate stack comprising  
a conductive oxide layer overlying the substrate selected from the group of materials consisting of:

an oxide of the formula AO<sub>x</sub>, where A is a material selected from the group consisting of Mo, W, Tc, ~~Re, Ru,~~ Os, Rh, Ir, Pd, ~~Pt,~~ In, Zn, Sn, Sr-Ru, Nd, Nb, Sm, La, V, and NaCl;

a perovskite oxide of the formula  $ABO_3$ , where A and B are a combination selected from the group consisting of (A = Ca, Sr)(B = V, Cr, Fe, Ru), (A = La)(B = Ti, Co, Ni, Cu), (A = H, Li, Na, K)(B = Re, Mo, Nb), and (A =  $La_{1-x}Sr_x$ )(B = V, Mn, Co);

a perovskite oxide of the formula  $A_2B_2O_7$ , where A and B are a combination selected from the group consisting of (A = Bi, Pd)(B =  $Ru_{1-x}Bi_x$ ,  $Ru_{1-x}Pb_x$ );

a layered perovskite oxide selected from the group consisting of  $CaTiO_3$ ,  $Ba_2RuO_4$ , and  $(Sr(Ru, Ir, Cr)O_8)(SrO)_N$ ; and

a high temperature superconducting oxide selected from the group consisting of  $La_{1-x}Sr_xCuO_4$ ,  $Nd_{1-x}Ce_xCuO_4$ ,  $YBa_2Cu_3O_7$ ,  $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ , and  $(Nd_{1-x}Ce_x)_2CuO_4$ ; and

a sacrificial layer over the conductive oxide layer;

forming drain and source regions on opposite sides of the replacement gate stack;

filling the areas surrounding the replacement gate stack while exposing the top portion of the replacement gate stack;

removing the sacrificial layer portion of the replacement gate stack;

forming the remainder of the gate stack, the remainder of the gate stack comprising

a ferroelectric material layer over the conductive oxide layer;

and

a top electrode conductive layer over the ferroelectric material layer.

14. (original) A method as in claim 13 wherein the replacement gate stack further comprises a bottom electrode conductive layer positioned between the conductive oxide layer and the sacrificial layer.

15. (original) A method as in claim 13 wherein the sacrificial layer material comprises silicon nitride or silicon dioxide.

16. (original) A method as in claim 13 wherein the filling of the areas surrounding the replacement gate stack while exposing a top portion of the replacement gate stack comprises  
the deposition of a dielectric film; and  
the planarization of the deposited dielectric film to expose the top portion of the replacement gate stack.

17. (original) A method as in claim 13 wherein the formation of the remainder of the gate stack comprises  
the deposition of the ferroelectric material layer;  
the planarization of the ferroelectric material layer;  
the deposition of the top electrode conductive layer;  
the photolithography patterning of the top electrode conductive layer; and  
the etching of the top electrode conductive layer.

18. (original) A method as in claim 13 wherein the formation of the replacement gate stack comprises the deposition of the

replacement gate stack, the photolithography patterning of the replacement gate stack and the etching of the replacement gate stack.

19. (original) A method as in claim 13 wherein the electrode conductive layer is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide.

20. canceled

21. (previously presented) A ferroelectric transistor comprising:

source, drain, and channel regions formed in a substrate;  
a gate structure including:

a conductive oxide layer overlying the channel region having a lattice structure;

a ferroelectric material layer overlying the conductive oxide layer having a lattice structure matching the conductive oxide lattice structure; and,

a top electrode conductive layer overlying the ferroelectric material layer.

22. (previously presented) The ferroelectric transistor of claim 21 wherein the gate structure further includes a bottom electrode conductive layer interposed between the conductive oxide layer and the ferroelectric material layer.

23. (previously presented) The ferroelectric transistor of claim 21 wherein the ferroelectric material layer has a perovskite crystal lattice structure.

24. (previously presented) A ferroelectric transistor comprising:

source, drain, and channel regions formed in a substrate;

a gate structure including:

a non-silicon-containing conductive oxide layer overlying the channel region;

a ferroelectric material layer overlying the conductive oxide layer; and,

a top electrode conductive layer overlying the ferroelectric material layer.

25. (previously presented) The ferroelectric transistor of claim 24 wherein the gate structure further includes a bottom electrode conductive layer interposed between the conductive oxide layer and the ferroelectric material layer.

26. (previously presented) A ferroelectric transistor consisting of:

source, drain, and channel regions formed in a substrate;

a gate structure including:

a conductive oxide layer overlying the channel region;



a ferroelectric material layer overlying the  
conductive oxide layer; and,  
a top electrode conductive layer overlying the  
ferroelectric material layer.

27. (previously presented) A ferroelectric transistor  
consisting of:  
source, drain, and channel regions formed in a substrate;  
a gate structure including:  
a conductive oxide layer overlying the channel  
region;  
a bottom electrode conductive layer overlying  
the conductive oxide layer;  
a ferroelectric material layer overlying the  
bottom electrode conductive layer; and,  
a top electrode conductive layer overlying the  
ferroelectric material layer.